Z-Set and Independent Fault Set based Fault Pair Collapsing for Fault List Reduction

Chinju.G, J.P.Anita

Abstract— In fault pair collapsing, certain fault pairs are eliminated from the fault list, since those fault pairs are guaranteed to be distinguished by the remaining fault pairs in the fault list. Considering a fault pair is important in the case of diagnostic fault simulation and test generation. The concept of Z-set and independent fault set are used for fault pair formation. Z-set characteristics determine the numbers of fault pairs that are guaranteed to be distinguished by a given fault detection test set. So the remaining fault pairs are considered for further fault pair collapsing process. Independent fault pairs are formed from the collapsed fault list such that each fault in that pair cannot be covered by the tests derived for another fault. For fault pair collapsing process, a fault pair is selected which is not included in the independent fault set. Hence a reduction in the number of fault pairs is obtained. Again to further reduce the numbers of fault pairs, dominance relations between the faults are considered.

Index Terms—Diagnostic test generation, Distinguishable fault pairs, Dominance and Equivalence in fault pairs, Fault pair collapsing, Fault Pair forming, Independent fault set, Z-set.

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1 Introduction

EQUIVALENCE and dominance relations between faults have been used for the diagnostic fault simulation, test generation as well as in the analysis of faulty circuit responses. The main aim of diagnostic test generation is to generate a test set that distinguishes the fault pairs. Fault pairs are considered directly or indirectly during these processes. For example, the diagnostic test generation is to ensure that for every pair of faults f_1 and f_2 there is at least one test t such that the circuit-under-test produces a different output response depending on whether f_1 or f_2 is present in the circuit.

The concepts of fault equivalence and fault dominance are used to reduce the number of faults targeted. This is referred to as fault collapsing. If two faults are equivalent, only one of them needs to be considered during test generation and fault simulation. If one fault is detected, the other one is guaranteed to be detected as well. Similarly, if a fault f_j dominates a fault f_i and f_i is detectable, only f_i needs to be considered during test generation. If f_i is detected, f_j is guaranteed to be detected as well.

In this work, the equivalence and dominance relations are defined where the basic entity is a fault pair and a collapsing process referred to as fault pair collapsing is done. Equivalence and dominance relations between fault pairs are defined [1] as follows. A fault pair is denoted by $p_i = (f_{i1}, f_{i2})$, let $T(p_i)$ be the set of all the tests that distinguish f_{i1} and f_{i2}.

Definition 1: Fault pairs $p_1 = (f_{11}, f_{12})$ and $p_2 = (f_{21}, f_{22})$ are equiv
alent, if $T(p_1) = T(p_2)$.

Definition 2: Fault pair $p_2 = (f_{21}, f_{22})$ dominates fault pair $p_1 = (f_{11}, f_{12})$ if $T(p_1) \subset T(p_2)$.

These definitions [1] are similar to the definitions of equivalence and dominance between single stuck-at faults.

In the proposed paper, the structural characteristics of a circuit like Z-set [3] and independent fault set [6] concept are used. This Z-set is helpful to determine the fault pairs that are guaranteed to be distinguished by a fault detection test. Z-set is defined as the set that contains every output such that there is a directed path from the line in the circuit to each output in that set. Independent fault [6] concept is also useful for reducing the number of fault pairs from the fault list. A new method is developed for determining independent fault set from the collapsed fault list. If two faults are said to be independent, then there is no common test vector for the detection of these two faults. If two faults f_1 and f_2 are considered as independent, then the fault pair (f_1, f_2) is guaranteed to be distinguished by a given diagnostic test set.

2 Previous Work

In earlier works, several faults collapsing technique are used to reduce the number of faults in the fault list. The graph model [2] is used to represent equivalence and dominance between the faults. If a fault f_2 dominates f_1 then this is represented by a directed edge from node f_1 to f_2. Similarly, equivalences can be denoted as edges from f_1 to f_2 and from f_2 to f_1.
It is observed that this method resulted in global fault collapsing, but is not useful for non Boolean gates like pass transistors and tri state devices. In Paper [7], a hierarchical approach to fault collapsing is used which resulted in an increased efficiency compared to the non hierarchical one. A new method for fault collapsing known as dominance with sub faults is introduced in [8]. In [3], Z-set and Z-detection are described for finding out distinguishable fault pairs in a circuit. In [5], a level of similarity is used to reduce the number of faults. This property is also applicable to fault pair collapsing that is described in paper [1]. Diagnostic fault simulation and its algo-

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rithm are explained in [4]. In paper [1], explained about fault pair collapsing process.

In the proposed work, a new technique of fault pair collapsing is done using independent fault set and Z-set. Hence the numbers of fault pairs are reduced when compared to the existing literature.

3 FAULT PAIR COLLAPSING

Fault pairs are considered instead of individual faults for fault collapsing process. Equivalence and dominance properties are defined for these fault pairs. Fig.1 shows an example circuit and it has two inputs and two outputs and the line numbers are written in square brackets.

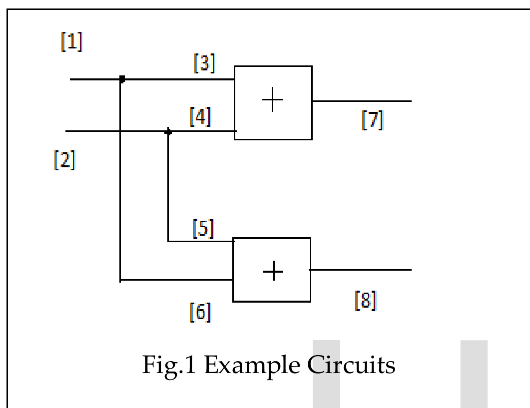

Fig.1 Example Circuits

Table 1 shows stuck-at fault corresponding to each line in the Fig.1 circuit. Four possible inputs are given in table and their corresponding fault free output is shown in first row. Stuck-at faults and their faulty outputs are given in the table.

TABLE 1
Single stuck-at faults

	Inputs			
	00	**01**	**10**	**11**
Fault free o/p	00	11	11	11
Faults	**Faulty o/p**			
3/0	00	11	01	11
4/1	10	11	11	11
5/0	00	10	11	11
6/1	01	11	11	11
8/1	01	11	11	11

Fault pairs are formed using these single faults. Some of the fault pairs of the example circuit are shown in the Table 2. All possible combinations of fault pairs are formed from the single faults in Table 1.Test vectors that distinguishes each fault in the pair are given in the third column.

TABLE 2
Fault Pair formation

i	Fault pair f_{i1}	f_{i2}	T(Pi)
P0	3/0	4/1	10,00
P1	3/0	5/0	10,01
P2	3/0	6/1	10,00
P3	3/0	8/1	10,00
P4	4/1	5/0	00,01
P5	4/1	6/1	00
P6	4/1	8/1	00
P7	5/0	6/1	01,00
P8	5/0	8/1	01,00
P9	6/1	8/1	00

Equivalence and dominance relations are easily found out from this Table 2. Test vectors for fault pairs P_0, P_2, and P_3 are the same, which means that they are equivalent. Similarly fault pairs P_7 and P_8 are also equivalent.

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3.1. Z-SET CHARACTERISTICS

Fault pairs can be also formed based on Z-set property. Z-set indicates that line in the circuit influence which primary output.

TABLE 3
Results of Z-set in benchmark circuits

Circuits	No. of distinct Z-set	Fault pairs based on Z-set
c17	3	70
c432	15	25298
c880	68	18359
s208	32	3128
s298	43	2063
s382	51	2372
s400	51	2744
s444	51	3507
s420	60	12713
s526	65	4738
s641	77	2630
s510	60	12797
s820	50	30444
s832	50	32980
b01	14	789
b02	9	314
b03	71	1763

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example, in c17 benchmark circuit has two primary outputs. Let the output be z_0 and z_1. Three distinct Z-set can be formed in c17. They are represented using vectors as 11, 01, and 10.If third line influences the first primary output, then their Z-set is $Z_3 = \{z_0\}$ (represented as 10). Based on Z-set characteristics, faults detected on the same outputs are paired and number of these type of fault pairs obtained for various benchmark circuits are shown in Table 3. So these fault pairs are used for further collapsing process.

Numbers of distinct Z-set states present in each circuit are shown in second column of Table 3. We got the reduced number of fault pairs compared to all possible fault pair combinations.

3.2. INDEPENDENT FAULT SET

Independent fault set is defined as one in which no two faults can be detected by the same test. This fault set is developed from collapsed fault list obtained from HOPE tool. Using the HOPE fault simulation tool, obtained a file which contained the faults and its corresponding test vectors. Comparing each test vector of two faults and if test vectors of two faults are not equal, then the faults are said to be independent.

4. EXPERIMENTAL RESULTS

In this section we present the experimental results of the proposed fault pair collapsing methods. The proposed method is implemented in the C language. Initially collapsed fault list is generated for various ISCAS and ITC'99 benchmark circuits. The fault pair collapsing process proceeds as follows.

Procedure: Fault pair collapsing process

1. Let F be the detectable collapsed circuit faults.
2. Find its Z-set Z (f) for every fault.
3. Determine the set of independent fault over F and fault pair is formed based on this set.
4. Set $P_{final} = \Phi$
5. Every pair of faults $f_1, f_2 \in$ F such that $Z(f_1) \cap Z(f_2) \neq \Phi$,if that pair f_1, f_2 not in independent set, then add the pair (f_1, f_2) to P_{final}.

The fault pairs based on the Z-set and independent fault set are obtained. In Table 3, third column showed the all possible number of fault pairs. Fault pairs are formed based on the independent fault concept. So a test vector must distinguish the faults in the independent fault set. Fault pairs are formed based on the Z-set property described in the procedure step 5.These results are shown in Table 3. So faults which are detected on the same output node were considered for fault pair formation. Because these fault pairs are not distinguished during the diagnostic test pattern generation.

Fault pairs which satisfied the Z-set property are again compared with the independent fault set. Fault pairs are selected in such a way that which is not contained in the independent set. These results are shown in Table 4.Here P_{final} denote the reduced number of fault pairs as compared to the initial fault pair.

TABLE 4
Number of fault pairs

Circuits	No. of all fault pairs	No. of independent fault pairs	P_{final}
c17	231	172	48
c432	137026	127196	13106
c880	443211	413167	10354
s208	23436	20995	1684
s298	47278	42987	1120
s382	79401	73254	1296
s400	89676	79310	1575
s444	112101	94572	1939
s526	153735	142841	2058
s641	106953	95547	1362
s420	92235	85993	6930
s510	158766	15022	4160
s820	360825	352508	14682
s832	378015	358098	16992
b01	6903	5778	442
b02	2016	1734	174
b03	77421	66853	918

Comparing the number of fault pairs P_{final} with the values in the existing literature are shown in Table 5.

TABLE 5
Comparison of number of fault pairs

Circuits	P_{final} [1]	P_{final} (Proposed)
s208	8.6E3	1684
s298	1.1E4	1120
s382	1.5E4	1296
s400	1.6E4	1575
s526	2.7E4	2058
s641	4.6E4	1362
s420	2.8E4	6930
s510	6.0E4	4160
s820	6.9E4	14682
b03	2.1E4	918

There is a huge reduction in the number of fault pairs obtained by the proposed method as compared to that in the existing literature.

5. CONCLUSION

The proposed work differs from the earlier works as the fault pairs are considered instead of individual faults for fault collapsing. Initially Z-set and independent fault are formed from collapsed single fault list. Fault pairs are formed based on the Z-set property and independent faults. A reduced numbers of fault pairs are obtained compared to the existing literature. A limitation to the proposed work is that simulation time is

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higher for larger benchmark circuits.

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